REMARKS

Claims 1-4, 6-11 and 16-24 were rejected and claims 5 and 12-15 were objected to in the June 1, 2005 Non-Final Office Action. Reconsideration and withdrawal of the rejections set forth in the Office Action is respectfully requested.

The applicant's representative wishes to thank the Examiner for the thorough office action, including the specific recitation of portions within the applied references with respect to certain claims, and for the indication of allowable subject matter.

Embodiments of the invention are first discussed, followed by discussion of the Cecchi reference and the Jeong reference. Next, distinctions between the rejected independent claims and the cited references are discussed.

I. Embodiments of the Claimed Invention

Embodiments of the claimed invention are directed to a system that connects a transmitter and receiver, or a transceiver, to a transmission line. The system determines the incoming signal by subtracting the outgoing signal (the "transmitter signal") from the signal on the transmission line (the "transmission line signal").

The system operates on differential signals rather than single-ended signals. A differential signal is conveyed on two lines rather than a single line. One line carries the positive polarity form of the signal, while the other line carries the negative polarity form of the same signal.

The system determines the difference between the transmitter signal and the transmission line signal using two differential amplifiers. The first subtracts the positive polarity signals, while the second subtracts the negative polarity signals. Common mode rejection in each of the differential amplifiers is controlled by bias signals generated in response to the differential amplifier's output voltage. The output differential signals are then input into an output amplifier that combines the positive and negative polarity signals

into a single-ended signal. The output amplifier is built with asymmetry in its transfer characteristic that filters out noise below a certain threshold. Finally, the output signal is input into a logic gate that controls the adverse effects of the asymmetry in the output amplifier by having a logic threshold voltage that is higher than the mid-supply voltage of the output amplifier.

II. The Cecchi Reference

The system of Cecchi is directed to a system to amplify a single differential signal and convert it into a single-ended signal. The system uses three differential amplifiers in two stages to amplify the signal to a communications receiver. The first stage uses two differential amplifiers to find the difference between the two polarities of the differential signal. The inputs to the amplifiers are reversed between the first and second differential amplifiers in this stage. This mechanism is used to balance out any inherent imbalances coming from differences in manufacture of the transistors. Common mode rejection in the differential amplifiers is controlled by feedback between different elements of the amplifiers. In the second stage of amplification, the output signals from the first stage are input into a third differential amplifier to produce a single-ended output signal.

III. The Jeong Reference

The system of Jeong is directed to a system for transmitting and receiving parallel data over a single serial line. The system converts outgoing parallel data to serial form and transmits it over a single serial line. It uses a two-way buffer to separate the incoming signal by subtracting the outgoing signal from the combined signal on the transmission line. The received data is then converted into parallel form and forwarded to the receiver.

IV. Cecchi does not teach the use of asymmetry to limit the effects of input noise

Claims 1-4, 6-11, 16-20 and 24 were rejected in whole or in part as being unpatentable over Cecchi (U.S. Patent No. 6,549,971) in view of Jeong. (U.S. Patent No.

5,675,584). Distinctions with claim 1 will be discussed, followed by application to the remaining independent claims.

Claim 1 recites a data communications system including a bi-directional buffer, where the buffer includes a differential amplifier that generates an output logic signal from a differential signal and filters out input noise by introducing asymmetry into the transfer characteristic. For example, where the transfer function for such a differential amplifier is centered around zero voltage, the transfer function will be centered around some other voltage, either greater or less than zero. The skewed transfer function then filters out input noise that is less than the size of the skew. The system uses this asymmetry in the transfer characteristic to avoid interpreting system noise as data.

The Office Action suggests that the asymmetry aspect of claim 1 is anticipated by Cecchi, which describes compensating for asymmetries inherent in the amplification stages. Applicants respectfully disagree. In fact, Cecchi teaches away from the Applicant's use of asymmetry. The cited portion in Cecchi, top of Col. 7, describes the system as intended to compensate for the problems caused by asymmetry. In particular, the system in Cecchi helps to compensate for asymmetries that arise from "mismatch of the effective channel lengths or saturated drain currents of the p-channel and n-channel devices in each amplification circuit." So, Cecchi describes asymmetry as a problem to be overcome. This is distinct from claim 1, which, as noted above, describes a system that instead actually uses asymmetry as a tool to eliminate the problem of input noise.

Jeong fails to make up for the deficiencies of Cecchi. Thus, applicants submit that claim 1 and dependent claim 2-4 are patentable over Cecchi and Jeong at least for the reasons above, and respectfully request the rejections be withdrawn.

Many of the remaining claims also describe similar elements to those in claim 1, including the element of "suppressing effects of input noise on the output logic signals by skewing an output amplifier transfer characteristic." Therefore, independent claims 19, 22

and 23, and claims which depend from them, are patentable over Cecchi for at least the reasons stated above, and applicants respectfully request the rejections be withdrawn.

V. The combination of Cecchi and Jeong does not render the claimed system unpatentable: Cecchi and Jeong cannot be combined, lack of motivation for them to be combined, fail to provide any reasonable expectation of success for their combination, and even if combined, fail to disclose the recited positive and negative polarity signals

The Office Action argues that Jeong can supplement Cecchi to teach the use of the difference between a positive polarity transmission line signal and a positive polarity transmission transmitter signal and the difference between a negative polarity transmission line signal and a negative polarity transmission transmitter signal. In particular, the subtraction of line signal and transmitter signal described in Jeong can be combined with the multi-stage differential amplifiers in Cecchi to teach the system described in claim 1. The proposed modification was to modify Cecchi to clarify that a transmission signal and a transmitter signal are known to the art. Applicants respectfully disagree with the proposed modification.

The two systems cannot be combined in the way proposed. As noted above, Cecchi describes a system that amplifies an input differential signal and outputs a single-ended signal based on the input signal. It is intended to amplify the signal at a receiver, rather than to serve as a two-way buffer. As such, it only receives a single signal. The Office Action incorrectly describes the input signal to the system in Cecchi as "differentiated." In fact, as noted above, the signal is a differential signal, meaning that a single signal is being transmitted by using two wires. If V1 and V2 in Cecchi were modified to be transmission line signal and transmitter signal as suggested, the input would no longer be a differential signal as required by Cecchi.

In addition, the cited motivation to combine Cecchi and Jeong is insufficient to justify the combination. First, the systems described serve different purposes. The system described by Cecchi is designed to allow a receiver to amplify a received signal to

compensate for various types of transmission losses that make it difficult to convert a differential signal to a single-ended CMOS signal. The goal is to enhance existing receiver circuits without significantly increasing the cost of those circuits. In contrast, the system described by Jeong is designed to allow "high speed conversion of parallel data to serial form and transmission over a serial link." The goal is to provide a less expensive means of converting parallel data to serial form and back. Although both systems are intended to be incorporated into communications systems, their purposes are significantly different and they would not be combined.

An additional sign of this difference in purposes is the difference in international classifications for the two patents. Cecchi was classified G06F, which is for "Electrical Digital Data Processing" in the general category of Physics. In contrast, Jeong was classified H04L, which is for "Transmission of Digital Data" in the general category of Electricity. This difference shows the different purposes of the two systems and suggests that a person skilled in the art would be unlikely to be motivated to combine them.

The argument that there would be a reasonable expectation of success is also inadequate. While in one embodiment the system described by Cecchi is connected to a I/O bus, there is no similar connection for the additional aspect taught by Jeong. The system in Jeong connects to a system bus with its parallel-to-serial converter. However, the two-way buffer that is the source of the addition to Cecchi is only connected to serial lines. For this reason, there would be no reasonable expectation of success in combining the two patents.

Even if Cecchi could be modified to take the transmission line signal and the transmitter signal, it would not render claim 1 unpatentable. Cecchi describes a system wherein the initial differential amplifiers receive the same signals as inputs, but with the order reversed in the second amplifier. Using the same signals with the order reversed is an important aspect of Cecchi's system, as it allows the system to "compensate[] for any asymmetries in the amplification stages..." (Cecchi, Col 7, Lines 19-20). In contrast, the

system recited in claim 1 uses four different signals input into the differential amplifiers. The first amplifier receives the positive polarity transmission line signal and the positive polarity transmitter signal. The second amplifier receives a different pair of signals, the negative polarity transmission line signal and the negative polarity transmitter signal. Therefore, even if Cecchi could be modified, it would still not receive all of the inputs that claim 1 describes. Jeong fails to make up for the deficiencies of Cecchi.

For these reasons, the combination of Cecchi and Jeong does not teach every element of claim 1. Applicants submit that claim 1 and dependent claims 2-4 are patentable over Cecchi in view of Jeong for at least the reasons stated above and respectfully request that the rejections be withdrawn.

Independent claims 6, 16-19 and 24 describe similar elements to those in claim 1, including the element of "subtract[ing] differential signals of the communication device from differential signals of the transmission line to generate a positive polarity difference signal and a negative polarity difference signal." Therefore, independent claims 6, 16-19 and 24 and dependent claims 7-11 and 20 are patentable over Cecchi in view of Jeong for at least the reasons stated above, and applicants respectfully request that the rejections be withdrawn.

VI. Cecchi does not describe using a bias signal based on the output common mode voltage to control common mode rejection

Using feedback to control common mode rejection in a differential amplifier is well-known in the art. However, there are patentable distinctions in the type of feedback in particular circuits. Cecchi describes an amplifier that incorporates a feedback stage as an intermediate step between the input and the output of the amplifier. For example, in Figure 2 of Cecchi, the feedback connections, 123 and 126, are connected to the intermediate voltage V1 at node 122. In contrast, claim 1 recites, inter alia, "using bias signals generated in response to an output common mode feedback voltage from the ... differential amplifiers." That is, the feedback in the claimed system is actually a separate

circuit that is controlled by the output of the differential amplifier. For example, as shown in Figure 4, the input to the feedback circuit 213 is the same as the output voltage 212a from the differential amplifier circuit. The feedback circuit then produces a bias voltage that controls the common mode rejection of the differential amplifier. Because of this difference in the method of controlling the common mode rejection, the claims should be allowed as patentable.

Applicants submit that claim 1 and dependent claims 2-4 are patentable over Cecchi for at least the reasons stated above and respectfully request that the rejections be withdrawn.

Independent claims 16, 19, 21, 23 and 24, as well as dependent claims 7-9, describe similar elements, including the element of "control[ling] common mode rejection in the differential amplifiers via bias signals generated in response to an output common mode feedback voltage..." Therefore, independent claims 16, 19, 21, 23 and 24 and dependent claims 7-9 and 20 are patentable over Cecchi and Jeong for at least the reasons stated above, and applicants respectfully request that the rejections be withdrawn.

VII. Claims 19, 20, 22 and 23 should have been allowed because they recite, in part, elements found in allowable claims 5 and 12-14

Claims 5 and 12-14 describe an aspect of the system where "symmetry is controlled in characteristics of the output logic signal using at least one logic gate with a higher logic threshold voltage than the mid-supply voltage...." The Examiner objected to these only because they were dependant on claims that were rejected.

Independent claims 19, 22 and 23 were rejected for reasons discussed above. However, they should have been allowed because they recite similar limitations to those found in allowable claims 5 and 12-14. Claims 19 and 22 describe methods that includes as a step "controlling symmetry in switching transients of the output logic signals by increasing a logic threshold voltage of a logic gate of the output amplifier above a mid-

supply voltage...." Similarly, claim 23 describes a computer readable medium that executes a process including the same step.

Applicants thus submit that independent claims 19, 22 and 23, and dependent claim 20, are patentable for at least the reasons stated above and respectfully request that the rejections be withdrawn.

VIII. Conclusion

Overall, independent claims 1, 6, 16-19 and 21-24 are patentable over the applied references. Since these independent claims are allowable, based on at least the above reasons, the claims that depend from them are likewise allowable. If the undersigned attorney has overlooked a relevant teaching in any of the references, the Examiner is requested to point out specifically where such teaching may be found.

In view of the foregoing, the claims pending in the application comply with the requirements of 35 U.S.C. § 112 and patentably define over the applied art. A Notice of Allowance is, therefore, respectfully requested. If the Examiner has any questions or believes a telephone conference would expedite prosecution of this application, the Examiner is encouraged to call the undersigned at (206) 359-3599. If the undersigned attorney has overlooked a relevant teaching in any of the references, the Examiner is requested to point out specifically where such teaching may be found.

Applicants believe no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 50-0665, under Order No. 120148004US3 from which the undersigned is authorized to draw.

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Respectfully submitted,

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